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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,601	05/31/2000	Kurt Eisenbeiser	CR00-001	2836

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EXAMINER

WILSON, SCOTT R

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 01/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/584,601

Applicant(s)

EISENBEISER ET AL

Examiner

Scott R. Wilson

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 November 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-10, 12 and 13 is/are rejected.
- 7) ☒ Claim(s) 7 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3, 4, 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

Art Unit: 2826

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of claims 1-13 in Paper No. 8 is acknowledged. The traversal is on the ground(s) that there is no explanation in the Restriction Requirement as to why the alleged "materially different product" is of such a different type and kind as to be considered "materially different", thereby supporting the restriction. This is not found persuasive because if the invention were embodied in the form of a MESFET, different gate dielectric materials, such as CeO_2 would be available, with correspondingly different electrical properties, rather than conventional JFET dielectrics, such as polysilicon, which can still be considered to be crystalline.

The requirement is still deemed proper and is therefore made FINAL.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: FET WITH AMORPHOUS GATE INSULATION LAYER.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2826

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizutani et al.. As to claim 1, Mizutani et al., Figure 1(g), discloses a semiconductor device comprising a semiconductor substrate (1) and a dielectric layer formed over the semiconductor substrate having a first portion (4) formed from SiO_2 , and a second portion (2) formed from monocrystalline CeO_2 (col. 3, line 48). The electric field in the dielectric layer, among other electric fields such as that from the gate (11), controls the conductivity of the semiconductor substrate. The SiO_2 layer (4) is formed by oxygen implantation followed by thermal annealing, which, although not explicitly stated, is known to those skilled in the art to form amorphous SiO_2 .

Claim 1 is also rejected under 35 U.S.C. 102(b) as being anticipated by IDS reference CM. Reference CM discloses a silicon substrate (1) covered by an amorphous SiO_2 layer (4) and further covered by an oxide of zirconium, yttrium or scandium (3).

Claim 1 is also rejected under 35 U.S.C. 102(b) as being anticipated by Mikami et al. (IDS reference DP). Mikami et al., in the abstract, discloses amorphous SiO_2 formed on a silicon substrate on which is grown an epitaxial single crystal film of $\text{MgO} \cdot \text{Al}_2\text{O}_3$.

Claim 1 is also rejected under 35 U.S.C. 102(b) as being anticipated by Chikyow et al. (IDS reference DR). Chikyow et al., in the abstract, discloses a $\text{CeO}_2/\text{SiO}_2/\text{Si}$ structure, in which the intermediate SiO_2 layer is amorphous, and the CeO_2 layer is a single-crystal insulating film lattice matched to the Si layer.

Art Unit: 2826

As to claim 2, Mizutani et al. discloses a control electrode (12) formed over the dielectric layer which establishes the electric field between itself and the semiconductor substrate.

As to claim 3, Mizutani et al. discloses a drain and source (9) and (10) where the electric field generates, in part, the conduction channel in the substrate which electrically connects the source and drain.

As to claim 4, Mizutani et al. discloses the first portion of the dielectric (4) formed adjacent to the semiconductor substrate (1), and the second portion of the dielectric (2) formed between the first portion and the control electrode (12).

As to claim 5, Mizutani et al. discloses the amorphous material to be SiO_2 .

As to claim 6, Mizutani et al. discloses that cerium or other rare earth elements, which would include lanthanum, may be used in the single crystal oxide insulation layer (col. 3, line 10).

As to claims 8 and 13, Mizutani et al. discloses the single crystalline CeO_2 layer to be 1000 Å in thickness (col. 3, line 49).

As to claim 9, Mizutani et al., Figures 3(d) through 3(g), discloses a transistor comprising a substrate (301), a gate electrode (324) disposed over the substrate for generating a conduction channel in the substrate in response to a control signal, and a dielectric, (321) and (302), formed over the conduction channel, the dielectric being formed with an amorphous SiO_2 layer (308), and a second layer formed with monocrystalline CeO_2 (302), disposed between the first layer and the gate electrode.

As to claim 10, Mizutani et al., Figure 3(g), discloses a source and drain (316) and (318) coupled electrically by the conduction channel.

Art Unit: 2826

As to claim 12, it is known by those skilled in the art that the relative permittivity of amorphous SiO_2 is 4.5, while the relative permittivity of monocrystalline CeO_2 is about 26 (Wang et al., Introduction).

Allowable Subject Matter


Claims 7 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is (703)308-6557. The examiner can normally be reached on M-F (8:30-4:30 Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703)308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-1782.

srw
December 28, 2001


SCOTT R. WILSON
Patent Examiner